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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,929	07/07/2003	Shigeyuki Aino	Q76416	6920

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EXAMINER	
MEHRMANESH, ELMIRA	
ART UNIT	**PAPER NUMBER**
2113	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/612,929	AINO ET AL.	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to an amendment filed on December 06, 2006 for the application of Aino et al., for an "Information processing apparatus" filed July 7, 2003.

Claims 19-37 are pending in the application.

Claims 19-37 are rejected under 35 USC § 102.

Claim 19 has been amended.

Claim 37 has been added.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 19-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Horst et al. (U.S. Patent No. 5,751,932).

As per claim 19, Horst discloses an information processing apparatus (col. 10, lines 29-32) comprising:

a first computer module (Fig. 1B, element 12A), which includes a controller (Fig. 2, element 26a) and a second computer module (Fig. 1B, element 12B), which includes another controller (Fig. 2, element 26a), wherein:

said each of said first and second computer modules includes a processor (Fig. 2, element 20b), a first memory (Fig. 2, element 28) and a second memory (col. 14,

lines 16-18, *cache memory*). Horst discloses cache memory (Fig. 2, element 22) could be used to supplement any cache memory that may be internal to the processor units (Fig. 2, element 20). Noting Fig. 29, a portion 28' of the memory space implemented by the memory 28 (Fig. 2) of a CPU 12. As Fig. 29 further illustrates, three cache boundaries CB_a, CB_b, and CB_c are contained with the memory portion 28', defining two cache blocks C_BLK_a and C_BLK_b (col. 41, lines 48-57).

said processors execute the same instructions substantially simultaneously and are substantially synchronized with each other (col. 16, lines 19-25)

said each first memory is read and written by the processor which is on the same computer module (col. 29, lines 62-67 through col. 30, lines 1-7)

said each second memory is read and written by the processor, which is on the same computer module (col. 29, lines 62-67 through col. 30, lines 1-7) and is written by said processor, which is on the second computer module (col. 16, lines 49-51)

wherein data is written to the first memory of the first computer module (col. 29, lines 62-67 through col. 30, lines 1-7) and the same data is written to at least the second memory of the first computer module. Horst discloses in duplex mode, careful handling of asymmetric variables is essential to ensure that *multiple copies of system memory* (maintained in the memory 28 of each CPU 12), assumed to be logically equivalent, *contain identical data* at all times (col. 71, lines 56-59)

wherein, during a normal process, first processor works by means of said first memory which is on the same computer module (Fig. 2) and said second memory is

written by said processor which is on the other computer module (col. 29, lines 62-67 through col. 30, lines 1-7)

wherein, during a rejoining process (col. 84, lines 56-58, *Reintegration*) first processor switches from working by means of said first memory which is on the first computer module to working by means of said second memory which is on the first computer module (col. 85, lines 15-46).

As per claim 20, Horst discloses each controller controls so that during the normal process read access from said processor which is on the same computer module is carried out as against said first memory which is on the same computer module and write access from said processor which is on the same computer module is carried out as against said first and said second memories which are on the same computer module and write access from said processor which is on the other computer module is carried out as against said second memory which is on the same computer module (col. 29, lines 62-67 through col. 30, lines 1-7).

and each controller controls so that, during the rejoining process, read access from said processor which is on the same computer module is carried out as against said second memory which is on the same computer module and write access from said processor which is on the same computer module is carried out as against said first and said second memory which are on the same computer module and said second memory which is on the other computer module (col. 85, lines 15-46).

As per claim 21, Horst discloses each controller copies the contents of said second memory which is on the same computer module to said first memory element which is on the same computer module when no read or write access from said processor which is on the same computer module to said second memory is present during the rejoining process (col. 29, lines 62-67 through col. 30, lines 1-7).

As per claim 22, Horst discloses each controller copies the contents of said second memory to said first memory by means of a direct memory access circuit (col. 16, lines 41-47).

As per claim 23, Horst discloses state of said computer module changes to the normal state from the rejoining state when the copy is completed for all memory areas of said second memory (col. 85, lines 15-46).

As per claim 24, Horst discloses state of said computer module changes to a normal state from the rejoining state when the copying is completed for all memory areas of said second memory (col. 85, lines 15-46).

As per claim 25, Horst discloses controllers are connected as a ring for three or more said computer modules (Fig. 1C) and (col. 13, lines 18-39).

As per claim 26, Horst discloses controllers are connected as a ring for three or more said computer modules (Fig. 1C) and (col. 13, lines 18-39).

As per claim 27, Horst discloses controllers are connected as a ring for three or more said computer modules (Fig. 1C) and (col. 13, lines 18-39).

As per claim 28, Horst discloses controllers are connected as a ring for three or more said computer modules (Fig. 1C) and (col. 13, lines 18-39).

As per claim 29, Horst discloses controllers are connected as a ring for three or more said computer modules (Fig. 1C) and (col. 13, lines 18-39).

As per claim 30, Horst discloses controllers are connected as a ring for three or more said computer modules (Fig. 1C) and (col. 13, lines 18-39).

As per claim 31, Horst discloses first and second computer modules are on lockstep fault tolerant computer system (col. 16, lines 19-25).

As per claim 32, Horst discloses first and second computer modules are on lockstep fault tolerant computer system (col. 16, lines 19-25).

As per claim 33, Horst discloses first and second computer modules are on lockstep fault tolerant computer system (col. 16, lines 19-25).

As per claim 34, Horst discloses first and second computer modules are on lockstep fault tolerant computer system (col. 16, lines 19-25).

As per claim 35, Horst discloses first and second computer modules are on lockstep fault tolerant computer system (col. 16, lines 19-25).

As per claim 36, Horst discloses first and second computer modules are on lockstep fault tolerant computer system (col. 16, lines 19-25).

As per claim 37, Horst discloses an information processing apparatus (col. 10, lines 29-32) comprising:

a computer module (Fig. 1B, element 12A) comprising a first processor (Fig. 2, element 20b), a first memory (Fig. 2, element 28) and a second memory (col. 29, lines 62-65)

a second processor apart from said computer module (Fig. 1B, element 12B) and executing the same instructions substantially simultaneously with said first processor (col. 16, lines 19-25)

wherein said first processor writes data to said first memory and said second processor writes said data to said second memory substantially simultaneously (col. 29, lines 62-67 through col. 30, lines 1-7)

and said first processor switches from reading said data from said first memory in a first state to reading said data from said second memory in a second state (col. 85, lines 15-46). Horst discloses reintegration is used to place two CPUs in duplex mode operation when first brought on line, or after operating in simplex mode for a time, or after a prior duplex mode operation of the system 10 resulted in a divergence, and the failing element (e.g., one of the CPUs) has been removed and replaced (col. 84, lines 65-67 through col. 85, lines 1-3).

Response to Arguments

Applicant's arguments filed December 06, 2006 have been fully considered but they are not persuasive. Refer to the corresponding section of the claim analysis for details.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).